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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/808,261	03/14/2001	Suraj J. Mathew	303.744US1	3364

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EXAMINER	
LATTIN, CHRISTOPHER W	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 02/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/808,261	MATHEW ET AL.	
	Examiner	Art Unit	
	Christopher W Lattin	2812	

-- The MAILING DATE of this communication app ars on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 November 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-50* is/are pending in the application.

4a) Of the above claim(s) *25-50* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-5 and 13-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rengarajan et al. (U.S. Patent 6,323,103) in view of Choi et al. (U.S. Patent 5,750,424) and Komori et al. (U.S. Patent 5,455,437).

In reference to claims 1-5, Rengarajan et al. teach a method of forming a gate dielectric layer 12 on the semiconductor substrate10, forming a first conductivity type semiconductor layer 14 on top of the first gate dielectric layer 12, over the second conductivity type semiconductor well 11, selectively removing a portion of the first conductivity type semiconductor layer 14 to expose the first gate dielectric 12, the portion defining a first conductivity type well region, forming a first conductivity type semiconductor well 30 in the first conductivity type well region, depositing a second conductivity type semiconductor layer 34 on a gate dielectric layer that is adapted for operation with a second conductivity type gate, and forming a second conductivity type gate 44 from the second conductivity type semiconductor layer 34 and forming source/drain regions 48 adjacent the gate, but fail to teach that the gate oxide is retained and not replaced following implantation. Choi et al. teach a method of forming a gate oxide 14, implanting ions through oxide 14 to form a well region and forming a

semiconductor gate layer on the oxide in order to reduce processing time. It would have been obvious to one skilled in the art at the time of the invention to use oxide 12 in Rengarajan et al. as a gate oxide in order to reduce processing steps, time and cost.

Although Rengarajan et al. in view of Choi et al. obviate forming an n-well 30 in a p well 10 comprised of the wafer, they fail to explicitly teach that a defined well of opposite conductivity lies below the well of first conductivity. Komori et al. teach a method of forming a well of one conductivity below a well of an opposite conductivity in order to isolate the device from the substrate and/or other devices. It would have been obvious to one skilled in the art at the time of the invention to form a well of opposite conductivity such as taught by Komori et al. below the well of first conductivity obviated by Rengarajan et al. in view of Choi et al. in order to isolate the device in the well of first conductivity in Rengarajan et al. from the substrate and other devices.

In reference to claims 13-17, Rengarajan et al. teach a method of forming a second conductivity type semiconductor well 11 in a semiconductor substrate 10, forming a gate dielectric layer 12 on the semiconductor substrate10, forming a first conductivity type semiconductor layer 14 on top of the first gate dielectric layer 12, over the second conductivity type semiconductor well 11, selectively removing a portion of the first conductivity type semiconductor layer 14 to expose the first gate dielectric 12, the portion defining a first conductivity type well region, forming a first conductivity type semiconductor well 30 in the first conductivity type well region, depositing a second conductivity type semiconductor layer 34 on a gate dielectric layer that is adapted for

operation with a second conductivity type gate, patterning and forming gates 42 and 44 from the first conductivity type semiconductor layer 14 and the second conductivity type semiconductor layer 34 and forming source/drain regions 48 and 52 adjacent the gates, but fail to teach that the gate oxide is retained and not replaced following implantation. Choi et al. teach a method of forming a gate oxide 14, implanting ions through oxide 14 to form a well region and forming a semiconductor gate layer on the oxide in order to reduce processing time. It would have been obvious to one skilled in the art at the time of the invention to use oxide 12 in Rengarajan et al. as a gate oxide in order to reduce processing steps, time and cost.

Rengarajan et al. in view of Choi et al. fail to teach that a well of opposite conductivity lies below the well of first conductivity. Komori et al. teach a method of forming a well of one conductivity below a well of an opposite conductivity in order to isolate the device from the substrate and/or other devices. It would have been obvious to one skilled in the art at the time of the invention to form a well of opposite conductivity such as taught by Komori et al. below the well of first conductivity obviated by Rengarajan et al. in view of Choi et al. in order to isolate the device in the well of first conductivity in Rengarajan et al. from the substrate and other devices.

Claims 6-12 and 18-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rengarajan et al. (U.S. Patent 6,323,103) in view of Komori et al. (U.S. Patent 5,455,437).

In reference to claims 6-12, Rengarajan et al. teach a method of forming a first gate dielectric layer 12 on a semiconductor substrate10, forming a first conductivity type semiconductor layer 14 on top of the first gate dielectric layer 12, selectively removing a portion of the first conductivity type semiconductor layer 14 to expose the first gate dielectric 12, the portion defining a first conductivity type well region, forming a first conductivity type semiconductor well 30 in the first conductivity type well region, removing the first gate dielectric layer 12 in the first conductivity type well region to expose a portion of the first conductivity type semiconductor well, forming a second gate dielectric layer 12' over the exposed portion of the first conductivity type semiconductor well 30 that is adapted for operation with a second conductivity type gate, depositing a second conductivity type semiconductor layer 34 on the second gate dielectric layer 12', and forming a second conductivity type gate 44 from the second conductivity type semiconductor layer and forming source/drain regions 48 adjacent the gate, but fail to teach that a well of opposite conductivity lies below the well of first conductivity. Komori et al. teach a method of forming a well of one conductivity below a well of an opposite conductivity in order to isolate the device from the substrate and/or other devices. It would have been obvious to one skilled in the art at the time of the invention to form a well of opposite conductivity such as taught by Komori et al. below the well of first conductivity taught by Rengarajan et al. in order to isolate the device in the well of first conductivity in Rengarajan et al. from the substrate and other devices.

In reference to claims 18-24, Rengarajan et al. teach a method of forming a second conductivity type semiconductor well 11 in a semiconductor substrate 10,

forming a first gate dielectric layer 12 on the semiconductor substrate10, forming a first conductivity type semiconductor layer 14 on top of the first gate dielectric layer 12, over the second conductivity type semiconductor well 11, selectively removing a portion of the first conductivity type semiconductor layer 14 to expose the first gate dielectric 12, the portion defining a first conductivity type well region, forming a first conductivity type semiconductor well 30 in the first conductivity type well region, removing the first gate dielectric layer 12 in the first conductivity type well region to expose a portion of the first conductivity type semiconductor well 30, forming a second gate dielectric layer 12' over the exposed portion of the first conductivity type semiconductor well that is adapted for operation with a second conductivity type gate, depositing a second conductivity type semiconductor layer 34 on the second gate dielectric layer 12', patterning and forming gates 42 and 44 from the first conductivity type semiconductor layer 14 and the second conductivity type semiconductor layer 34 and forming source/drain regions 48 and 52 adjacent the gates, but fail to teach that a well of opposite conductivity lies below the well of first conductivity. Komori et al. teach a method of forming a well of one conductivity below a well of an opposite conductivity in order to isolate the device from the substrate and/or other devices. It would have been obvious to one skilled in the art at the time of the invention to form a well of opposite conductivity such as taught by Komori et al. below the well of first conductivity taught by Rengarajan et al. in order to isolate the device in the well of first conductivity in Rengarajan et al. from the substrate and other devices.

Response to Arguments

Applicant's arguments filed 11/03/03 have been fully considered but they are not persuasive. Applicant has amended the independent claims to include as a limitation that the second conductivity type semiconductor well is sized to accommodate at least one transistor outside the first conductivity well region. Rengarajan et al. teach forming an n-well 30 in a p well 10 comprised of the wafer, which comprises another transistor 24A. Furthermore, Komori et al. teach forming wells of one conductivity within wells of other conductivities in order to isolate the devices. Contrary to applicant's assertions Komori et al. teach that the underlying region 22 can contain at least one additional transistor, Pch Tr, outside the first conductivity well region 4.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher Lattin whose telephone number is (703) 305-3017. The examiner can normally be reached Monday through Friday from 8:00 A.M. to 5:00 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling, can be reached at (703) 308-3325. The fax numbers for this Group are (703) 872-9318 for responses to non-final actions and (703) 872-9319 responses to final actions.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

CWL
February 2, 2004

John F. Niebling
Supervisory Patent Examiner
Technology Center 2800